Amendments

***In the Claims*:**

Please **ADD** claims 18-34 as shown in the following listing of the claims.

1. (Original) A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having a first contact window exposing the gate pad, and an opening portion partially exposing the insulating substrate;

a semiconductor pattern formed on the gate insulating layer;

a contact pattern formed on the semiconductor pattern;

a data line assembly formed on the contact pattern with substantially the same outline as the contact pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrode while being separated from the source electrodes;

a passivation layer formed on the data line assembly with the same outline as the semiconductor pattern except at portions of a second contact window exposing the data pad and a third contact window exposing the drain electrode;

a pixel electrode formed at a pixel area defined by the neighboring gate and data lines, the pixel electrode being electrically connected to the drain electrode through the third contact window while partially contacting the gate insulating layer; and

subsidiary gate and data pads contacting the gate and data pads, respectively.

2. (Original) The thin film transistor array substrate of claim 1 wherein the opening portion exposes the substrate between the pixel electrode and the neighboring data line.

3. (Original) The thin film transistor array substrate of claim 1 wherein the third contact window exposing the drain electrode is extended such that the borderline of the drain electrode is exposed to the outside.

4. (Original) A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source electrodes;

a second insulating layer formed on the data line assembly with the same outline as the semiconductor pattern, the second insulating layer having a second contact window exposing the gate pad through the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

5. (Original) The thin film transistor array substrate of claim 4 further comprising a contact layer formed between the semiconductor pattern and the data line assembly with the same outline as the data line assembly.

6. (Original) The thin film transistor array substrate of claim 4 further comprising subsidiary gate pads and subsidiary data pads covering the gate pad and the data pad, respectively.

7. (Original) The thin film transistor array substrate of claim 4 further comprising a photo-interceptive organic pattern formed between the data line assembly and the overlying passivation layer.

8. (Original) The thin film transistor array substrate of claim 7 wherein the photo-interceptive pattern is provided with a fifth contact window exposing the drain electrode

through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

9. (Original) The thin film transistor array substrate of claim 4 wherein the second insulating layer is formed with a photo-interceptive organic layer.

10. (Original) The thin film transistor array substrate of claim 9 wherein the first insulating layer has the same outline as the semiconductor pattern.

11. (Original) The thin film transistor array substrate of claim 10 wherein the opening width of the semiconductor pattern between the neighboring data lines is 1 μm or more.

12. (Original) A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source

electrodes, the data line assembly substantially having the same outline as the semiconductor pattern except the portion placed between the source electrode and the drain electrode;

a second insulating layer formed on the data line assembly, the second insulating layer having a second contact window exposing the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed on the passivation layer at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

13. (Original) The thin film transistor array substrate of claim 12 further comprising a contact layer formed between the semiconductor pattern and the data line assembly substantially with the same outline as the data line assembly.

14. (Original) The thin film transistor array substrate of claim 12 further comprising subsidiary gate pads and subsidiary data pads covering the gate pads and the data pads, respectively.

15. (Original) The thin film transistor array substrate of claim 12 further comprising a photo-interceptive organic pattern formed on the passivation layer over the data line assembly and the gate line assembly.

16. (Original) The thin film transistor array substrate of claim 15 wherein the photo-interceptive organic pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

17. (Original) The thin film transistor array substrate of claim 12 wherein the second insulating layer is formed with a photo-interceptive organic layer.

18. (Currently Added) A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes connected to the gate lines, and gate pads connected to end portions of the gate lines;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having a first contact window exposing the gate pad, and an opening portion partially exposing the insulating substrate;

a semiconductor pattern formed on the gate insulating layer;

a contact pattern formed on the semiconductor pattern;

a data line assembly formed on the contact pattern with substantially the same outline as the contact pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes connected to the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrode while being separated from the source electrodes;

a passivation layer formed on the data line assembly with the same outline as the semiconductor pattern except at portions of a second contact window exposing the data pad and a third contact window exposing the drain electrode;

a pixel electrode formed at a pixel area defined by the neighboring gate and data lines, the pixel electrode being electrically connected to the drain electrode through the third contact window while partially contacting the gate insulating layer; and

subsidiary gate and data pads contacting the gate and data pads, respectively.

19. (Currently Added) The thin film transistor array substrate of claim 18 wherein the opening portion exposes the substrate between the pixel electrode and the neighboring data line.

20. (Currently Added) The thin film transistor array substrate of claim 18 wherein the third contact window exposing the drain electrode is extended such that the borderline of the drain electrode is exposed to the outside.

21. (Currently Added) A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes connected to the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes connected to the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the

source electrodes with respect to the gate electrodes while being separated from the source electrodes;

a second insulating layer formed on the data line assembly with the same outline as the semiconductor pattern, the second insulating layer having a second contact window exposing the gate pad through the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

22. (Currently Added) The thin film transistor array substrate of claim 21 further comprising a contact layer formed between the semiconductor pattern and the data line assembly with the same outline as the data line assembly.

23. (Currently Added) The thin film transistor array substrate of claim 21 further comprising subsidiary gate pads and subsidiary data pads covering the gate pad and the data pad, respectively.

24. (Currently Added) The thin film transistor array substrate of claim 21 further comprising a photo-interceptive organic pattern formed between the data line assembly and the overlying passivation layer.

25. (Currently Added) The thin film transistor array substrate of claim 24 wherein the photo-interceptive pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

26. (Currently Added) The thin film transistor array substrate of claim 21 wherein the second insulating layer is formed with a photo-interceptive organic layer.

27. (Currently Added) The thin film transistor array substrate of claim 26 wherein the first insulating layer has the same outline as the semiconductor pattern.

28. (Currently Added) The thin film transistor array substrate of claim 27 wherein the opening width of the semiconductor pattern between the neighboring data lines is 1 μm or more.

29. (Currently Added) A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes connected to the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes connected to the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source electrodes, the data line assembly substantially having the same outline as the semiconductor pattern except the portion placed between the source electrode and the drain electrode;

a second insulating layer formed on the data line assembly, the second insulating layer having a second contact window exposing the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed on the passivation layer at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

30. (Currently Added) The thin film transistor array substrate of claim 29 further comprising a contact layer formed between the semiconductor pattern and the data line assembly substantially with the same outline as the data line assembly.

31. (Currently Added) The thin film transistor array substrate of claim 29 further comprising subsidiary gate pads and subsidiary data pads covering the gate pads and the data pads, respectively.

32. (Currently Added) The thin film transistor array substrate of claim 29 further comprising a photo-interceptive organic pattern formed on the passivation layer over the data line assembly and the gate line assembly.

33. (Currently Added) The thin film transistor array substrate of claim 32 wherein the photo-interceptive organic pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

34. (Currently Added) (The thin film transistor array substrate of claim 29 wherein the second insulating layer is formed with a photo-interceptive organic layer.